REMARKS

Claims 1-28 are pending in this application.

In paragraphs 1 and 2 of the office action, the Examiner rejects claims 1-27 under 35 USC §103(a) as being unpatentable over US patent no. 4,785,463 (Janc) in view of US patent no. 6,445,229 (Schenck). The applicant respectfully submits that the cited references do not disclose all the limitations of claim 1, and therefore the Examiner has not made a prima facie case of obviousness.

In making this rejection, the Examiner finds the following aspects of claim 1 in Janc:

1.	a method of generating at least two modulation signals from a local oscillator signal	fig. 8
2.	delaying	fig. 8 #878 col. 17, lns. 35-67
3.	the local oscillator signal	fig. 8 #846 col. 17, ln. 21 col. 18, lns. 20-31
4.	first modulation signal second modulation signal	fig. 8 #802 fig. 8, #822

However, the applicant believes that the cited figures and sections do not disclose the limitations of claim 1, and are better characterized as described below. As to number 1 above, the Examiner states that the preamble portion "a method of generating at least two modulation signals from a local oscillator signal ..." is disclosed in fig. 8. Although the preamble is not considered a limitation of the claim, the applicant submits that fig. 8 discloses a method and structure substantially different from the claimed invention. For example, as characterized by the Examiner, fig. 8 has first and second modulation signals (802 & 822). However, the textual notes next to 802/822 state that these signals are generated by the DSP 110, not by a local oscillator as recited in claim 1. Since

theses signals are generated by the DSP, and not "from a local oscillator signal", fig. 8 does not disclose "a method of generating at least two modulation signals from a local oscillator signal ...".

As to number 2 above, #878 in fig. 8 is shown as a "delay-lock Loop LPF". The inputs to #878 are described at Janc col. 17, lns. 29-35, which is duplicated below:

> The in-phase prompt and differential signals output from filters **808** and **828**, respectively, are multiplied together by mixer **872**. The corresponding quadrature signals output from filters **810** and **830** are multiplied by mixer **874**. The products of mixers **872** and **874** are summed by adder **876**, whose output is coupled to delay-locked loop (DLL) lowpass filter **878**.

As described in the duplicated section above, block 878 does not perform a step of "delaying the local oscillator signal", but instead accepts inputs downstream from the mixing process. According, the step of "delaying the local oscillator signal" is not disclosed in Janc. Further, the output of #878 is described at Janc col. 17, lns. 35-41, which is duplicated below:

> The signal output from DLL filter **878** represents the receiver-derived estimate of relative C/A code delay, which is sent to μP **114** for navigation calculations, via bus interface **882** and bus **750**. The code delay signal is also sent via switch **880** (position 0) to the code control input of the appropriate C/A code generator of DSP **110**.

As described in the duplicated section above, block 878 does not "form at least two sets of modulator signals" as recited in claim 1; instead it outputs a C/A code for use by a microprocessor. Again, Janc fails to disclose this limitation of claim 1.

As to number 3, above, the Examiner identifies #846 as the local oscillator signal. As shown in fig. 8, signals 846a and 846b are generated by block 846, and received directly into the complex mixers 802/822. There is no indication in fig. 8 of any process or structure for "delaying the local oscillator signal", as recited

in claim 1. Also, the cited portions of Janc also fail to even discuss any delaying of signals 846a or 846b. Instead, col. 17, ln. 21 merely states that the VFO 846 has sine and cosine outputs, while col. 18, lns. 20-31 states that the VFO receives a Doppler estimate at port 846d. In this way, fig. 8 and the cited portions do not disclose "delaying the local oscillator signal" as recited in claim 1.

As to number 4 above, the Examiner identifies a first and second modulation signal with reference to elements 802 and 822 of fig. 8. However, these elements do not show "one of said sets of modulator signals together forming the first modulation signal" or "another of said sets forming the second modulation signal". Instead, element 802 receives "prompt signals" from DSP 110, and receives signals 846a/b from VFO 846. And, the output from 802 is not a "modulation signal" at all, but is an I/Q signal, as described in Janc, col. 16, lns. 16-25:

> . In effect, complex mixer **802** performs a complex multiplication of the two "complex" signals PI+jPQ and cos ϕ+j sin ϕ. The product resulting from this multiplication comprises two output signals: an in-phase ("real") component {PI cos ϕ−PQ sin ϕ}, and a quadrature ("imaginary") component {PI sin ϕ+PQ cos ϕ}. These signals are applied to AGC amplifiers **804** and **806**, respectively, which serve to scale the signals to relatively constant average power level, thereby mitigating the effects of signal fading.

Thus, neither any input nor any output from 802/822 can be considered to disclose "one of said sets of modulator signals together forming the first modulation signal" or "another of said sets forming the second modulation signal".

Schenck, the secondary reference cited by the Examiner, does not overcome the deficiencies discussed above. For example, Schenck does not address quadrature subharmonic modulation as recited in claim 1. Instead, Schenck merely "provides a clock multiplier circuit" (Schenck, col. 1, lns. 46-48).

Since Janc and Schenck, either alone or in combination, fail to disclose all the elements of claim 1, the applicant respectfully submits that Janc and Schenck cannot render claim 1 obvious. In a similar manner, claims 2-9, which depend from claim 1, also cannot be rendered obvious.

For reasons as discussed above, the applicant respectfully submits that Janc and Schenck, either alone or in combination, fail to disclose all the elements of claim 10, and therefore cannot render claim 10 obvious. In a similar manner, claims 11-18, which depend from claim 10, also cannot be rendered obvious.

For reasons as discussed above, the applicant respectfully submits that Janc and Schenck, either alone or in combination, fail to disclose all the elements of claim 19, and therefore cannot render claim 19 obvious. In a similar manner, claims 20-27, which depend from claim 19, also cannot be rendered obvious.

In paragraphs 3 and 4 of the office action, the Examiner rejects claim 28 under 35 USC §102(b) as being anticipated by US patent no. 5,053,717 (Schulz). However, the applicant respectfully submits that Schulz fails to disclose the "quadrature amplitude modulated signal" as recited in claim 28. Instead, Schulz confines itself to FM demodulators. *See Schulz, col. 1, lns. 8-10.* Since Schulz fails to disclose all the limitations of claim 28, the applicant submits that Schulz cannot anticipate claim 28.

CONCLUSION

Applicant respectfully submits that pending claims 1-28 are now in a condition for allowance. If the Examiner would find it useful, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,

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